



Mobile Intel® Pentium® 4 Processor-M and Intel® 852PM/GME/GMV Chipset Platform

Design Guide Update

April 2005

Notice: The Intel® 852PM/GME/GMV chipset families may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

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Revision History

Revision Number	Description	Revision Date
-001	Initial Release	December 2004
-002	Updates Include: <ul style="list-style-type: none"> o Clarification on USB ESD protection 	March 2005

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Preface

This Design Guide Update document is an update to the specifications and information contained in *Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms Design Guide*, Document Number 253026. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2003. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types. However, only the detail for new material is included in this document. Both the public design guide document and this design guide update document are required to allow the users to have a complete list of information types and the associated details. This design guide update document will contain information that has not been previously published.

Affected Documents

Document Title/Document Number/	Document Location
<i>Intel® 852GME, Intel® 852GMV and Intel® 852PM Chipset Platforms Design Guide</i> , 253026-004	http://www.intel.com/design/mobile/desguide/253026.htm

Related Documents

Document Title	Document Location
<i>Intel® 852GME Chipset GMCH and Intel® 852PM Chipset MCH Datasheet</i>	http://www.intel.com/design/chipsets/datashts/253027.htm
<i>Intel® 82801DB I/O Controller Hub 4 Mobile (ICH4-M) Datasheet</i>	http://www.intel.com/design/mobile/datashts/252337.htm

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 852GM chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Tables of Changes

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Considerations in this Design Guide Update revision

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	Correction on pin-out/connection for Processor power

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Clarification on USB ESD protection

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General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

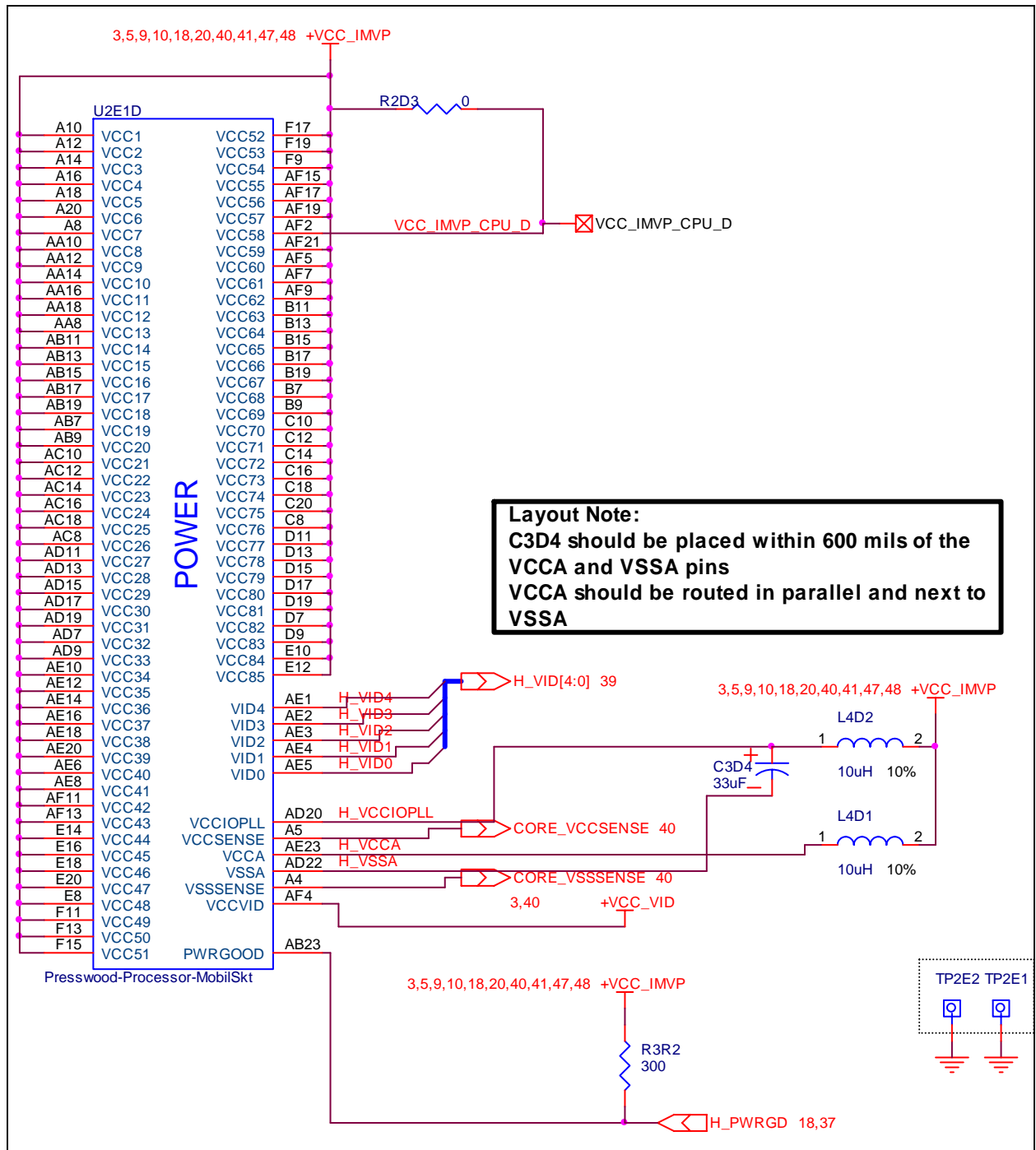
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Schematic, Layout, and Routing Updates

1. Correction on Pinout/Connection for Processor Power

Schematics net connections for VCCA and VCCIOPLL for the processor power should be corrected as follows (schematics sheet 4).



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Documentation Changes

1. Clarification on USB ESD Protection

Added reference to USB ESD Application Note.

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. [ESD protection is needed for USB lines. Refer to the Intel® ICH Family USB ESD Considerations Application Note for ESD protection implementation guidelines.](#) A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common-mode choke and the USB connector data pins as shown in Figure 108. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, Intel recommends including footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

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